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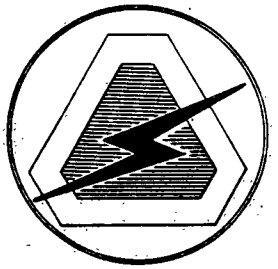
USAELRDL Technical Report 2330

CONTROLLED VARIATION OF DIFFUSED PHOSPHOROUS CONCENTRATION FOR SILICON PNP TRANSISTORS

Armand P. LaRocque

Nicholas O. Korolkoff



February 1963

UNITED STATES ARMY
ELECTRONICS RESEARCH AND DEVELOPMENT LABORATORY
FORT MONMOUTH, N.J.

U. S. ARMY ELECTRONICS RESEARCH AND DEVELOPMENT LABORATORY
FORT MONMOUTH, NEW JERSEY

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CONTROLLED VARIATION OF DIFFUSED PHOSPHOROUS CONCENTRATION FOR SILICON PNP TRANSISTORS

Armand P. LaRocque
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ABSTRACT

A method for diffusing phosphorous into silicon in order to achieve various surface concentrations has been developed. This method utilizes the phosphorous source temperature as a means of controlling the surface concentration over a range of 1×10^{17} to 5×10^{19} atoms per cc. Experiments were conducted over a source temperature range of 140°C to 240°C during a predeposition stage, at constant time and wafer temperature, followed by redistribution at constant time and temperature.

The predeposition source temperature is shown to affect the initial sheet resistance, ultimate sheet resistance and phosphorous concentration without materially affecting the junction depth.

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CONTROLLED VARIATION OF DIFFUSED PHOSPHOROUS CONCENTRATION FOR SILICON PNP TRANSISTORS

INTRODUCTION

In the design and development of solid state devices it is imperative that the device fabrication capability include processes for diffusing both donor and acceptor atoms over a wide range of dopant concentrations. A process for achieving control of one of the acceptor atoms (boron) has already been reported from these laboratories.[1]

The objective of the experiments described in this report was the development of a process which would permit controlled variation in the concentration of a donor atom. Phosphorous was chosen because of its favorable diffusion coefficient,[2] because the vapor pressure of a suitable source, phosphorous pentoxide, permitted its use over a satisfactory temperature range, and because the diffusion of phosphorous can be inhibited by the use of silicon dioxide layers on the silicon surface; a consideration important in the formation of localized diffused junctions in solid state devices.

THEORETICAL DISCUSSION

Fick's Second Law gives the relationship of diffusant concentration, c, diffusion time, t, and diffusion distance, x, as follows:

$$\frac{\partial c}{\partial t} = D \frac{\partial^2 c}{\partial x^2} \qquad (1)$$

where

D is the diffusion coefficient in cm^2/sec and is constant at a given temperature with which c, t and x are concerned.

The diffusion coefficient, D, varies with temperature as follows:

$$D = D_o \exp(-\Delta H/RT) \qquad (2)$$

where

D_o = diffusion constant in cm^2/sec
ΔH = diffusion activation energy in calories
R = gas constant in cal/degree
T = absolute temperature.

The value of D for phosphorous has been reported by Fuller and Ditzenberger as $10.5 \exp - (85{,}000/RT)$ over a temperature range of 1000^oC to 1400^oC.[2] Tannenbaum has shown that the diffusion coefficient at a constant temperature is constant up to concentrations of diffusant atoms of about 10^{20} cm^{-3} and increases rapidly at higher concentrations.[3] The phosphorous concentrations obtained in these experiments are all below this maximum so the diffusion coefficient can be assumed to have been constant.

There are three major distribution functions governing the inward diffusion of impurities into a solid:

1. Error function distribution: $N_x = N_s \operatorname{erfc}\left(\frac{x}{2(Dt)^{1/2}}\right)$ (3)

2. Gaussian distribution: $N_x = N_s \exp\left(\frac{-x^2}{4\,Dt}\right)$ (4)

3. Exponential distribution: $N_x = N_s \exp\left(\frac{-vx}{D}\right)$ (5)

where

N_x = impurity concentration at junction in atoms/cc
N_s = impurity concentration on the surface in atoms/cc
x = junction depth in centimeters
D = diffusion coefficient in cm^2/sec
t = time in seconds
v = surface recession rate in cm/sec.

The form of actual impurity distributions can be calculated from the differential equation subject to certain initial conditions and certain boundary conditions. The initial conditions are specified by the spatial dependence of the impurity concentration at time zero, while the boundary conditions specify conditions for the concentration or the flow of impurities at certain points or planes.[4] A great variety of diffused distributions is obtainable by the inward diffusion of impurities from the surface. For this, the impurities have to be introduced from some external phase which determines the concentration of the impurities in the solid. Smits[4] has described various surface phases such as the alloy source, reaction phase, vapor source two temperature systems, and a prediffusion phase.

It is the prediffusion phase which is most pertinent to the process under consideration. Under this technique the surface concentration can be controlled by the temperature of the source material and the carrier gas composition. The prediffusion (or predeposition) step, carried out at a relatively low temperature during these experiments, produced thin layers with high surface concentrations. It should be noted that in these experiments the resulting thin layers had sheet resistance values inversely related to the source temperature, as would be expected. Upon completion of the redistribution, or main diffusion, the deeper diffused layers had sheet resistance values directly related to the initial sheet resistance values. These relationships will be given in detail in a later section of this report. When the final layer thickness is deep compared to the thickness obtained in the predeposition, as was the case in these experiments, the impurity concentration essentially follows a Gaussian distribution, as given by Eq.(4).

EXPERIMENTAL PROCEDURE

Diffusion of Test Wafers

The method developed for controlling the variation of phosphorous

concentration in silicon was essentially a two-step procedure, namely a predeposition followed by a redistribution. The experimental diffusion system used for the predeposition step was similar to that reported by Frosch and Derick[5] and is shown in Fig. 1. It was essentially a long quartz tube enclosed in two separately controlled heating chambers. The source was placed within the lower temperature chamber while the silicon wafers were placed in the high temperature zone. Prior to the predeposition step, the silicon wafers, which were one Ω-cm p-type grown in the <111> plane, were cleaned according to a schedule previously reported from these laboratories.[6] The predeposition was carried out by heating a phosphorous pentoxide source at the desired temperature. Three grams of the source material were placed in a quartz boat, the temperature of which was constantly monitored by a thermocouple. Every effort was made to prevent absorption of atmosphoric moisture by the source material. Pure oxygen gas, which was dried in a series of liquid nitrogen traps and a Linde Molecular Sieve, was passed over the source at a rate of 1000 cc/min. The liquid nitrogen level was maintained low enough to minimize condensation of the oxygen. Upon insertion of the source boat, both the source and the furnace were allowed to stabilize for ten minutes before insertion of the wafer-holding boat into the higher temperature chamber from the other tube end. This avoided deposition of any initial high concentration burst of source material upon the wafers. Upon insertion of the wafers, the system was allowed to proceed at the desired temperatures for one hour.

Following removal of the silicon wafers, the silico-phosphorous glass surface film was removed by dissolution in hot acqua regia for five minutes followed by a rinse in hot, high resistivity water and a five minute rinse in hot sulfuric acid with another hot water rinse. Finally, the wafers were soaked in concentrated hydrofluoric acid, rinsed in hot water and blotted on lint-free paper. The wafers were then heated at 1200°C for one hour in an atmosphere of wet oxygen obtained by passing oxygen through high resistivity water held at 90°C. The diffused surface sheet resistance values were obtained by four-point probe measurements, and the junction depths were determined in the conventional manner of angle lapping, staining, and microscopic measurement.

Diffusion of Device Wafers

In addition to the aforementioned diffusions, this technique was used to prepare N-P planar diodes and the base region in planar P-N-P transistors. In order to effect localized junction regions, the wafers were oxidized to provide a mask against the phosphorous and windows formed in the desired location and pattern by photolithography. These processes, together with all other processes used to fabricate P-N-P transistors, have already been reported in detail.[6] In the case of phosphorous diffused diodes and base regions the wafers were cleaned, after the predeposition, in aqua regia and sulfuric acid, as given above, and were then partially etched in five percent hydrofluoric acid solution for 6-8 minutes in order to remove the masking oxide down to approximately 1000 Å. This eliminated the danger of there remaining any phosphorous source in the oxide in between the desired localized diffused regions.

RESULTS

Discussion of Diffusion Data

The test data, relating the predeposition source temperature and the resulting diffused film sheet resistance with the final sheet resistance, junction depth, and phosphorous concentration obtained following redistribution, are given in Table I. The dependence of the prediffused layer sheet resistance on the source temperature is shown in Fig.2. The relationship between the predeposited layer sheet resistance, an indication of dopant atomic concentration, and the ultimate diffused layer dopant concentration is given in Fig.3. The final relationship, namely that of the diffused dopant concentration with the source temperature during the predeposition step, is shown in Fig.4.

Examination of the data in Fig.2 discloses the anomalous sheet resistance values obtained at the lower source temperatures. This is believed due to the extreme difficulty in measuring such high sheet resistances over large wafer areas. The curve is therefore discontinuous to indicate the considered lack of reliable experimental data. That portion of the curve in Fig.3 which is concerned with the aforementioned anomalous values is also discontinuous.

Discussion of Device Electrical Test Data

The reverse breakdown characteristic of a typical diode, formed by diffusing at 1200°C for two hours following a predeposition at 700°C with a source temperature of 170°C, is shown in Fig.5. It is interesting to note that the breakdown voltage was 88 volts, an exceptionally high value for a diode formed in 1 ohm-cm p-type silicon. This is believed due to the extremely shallow diffusion gradient formed when a junction is formed at approximately 4.5 microns with a surface concentration of 10^{17} atoms per cc. This shallow gradient causes the formation of a compensated region immediately inside the junction so that the silicon is rendered effectively a high resistivity material.

The dc current gain, Beta, of a high frequency PNP planar transistor formed with a phosphorous base diffusion is shown in Fig.6. The collector current and step selector values were chosen to represent a Beta of 50 per division, so it can be seen that this transistor has a Beta value of approximately 85. The F_T value, namely the frequency at which the grounded emitter current gain becomes unity, was 425 MCS.

CONCLUSIONS

From an examination of the experimental data, it can be concluded that the phosphorous concentration of a diffused region in silicon can be varied over a range of about 4×10^{17} to 4×10^{19} atoms per cc. by a controlled variation of the phosphorous source temperature over a range of 185 to 215°C.

Thermally grown silicon dioxide is an effective mask against

phosphorous diffusion. This diffusion technique, together with this masking characteristic and photoresist, should permit the formation of diffused resistors over a wide range of values for use in solid state integrated circuits.

ACKNOWLEDGMENT

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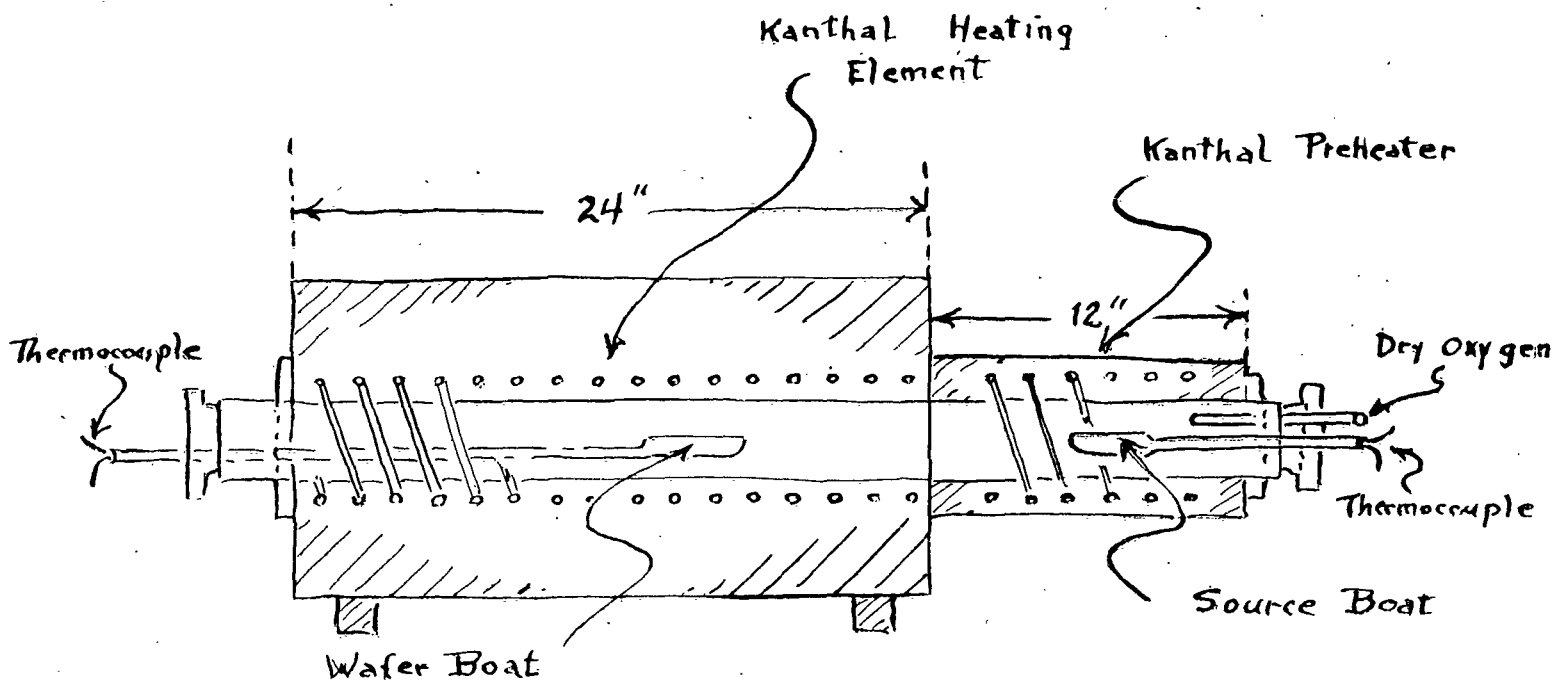


Fig. 1
DIFFUSION FURNACE

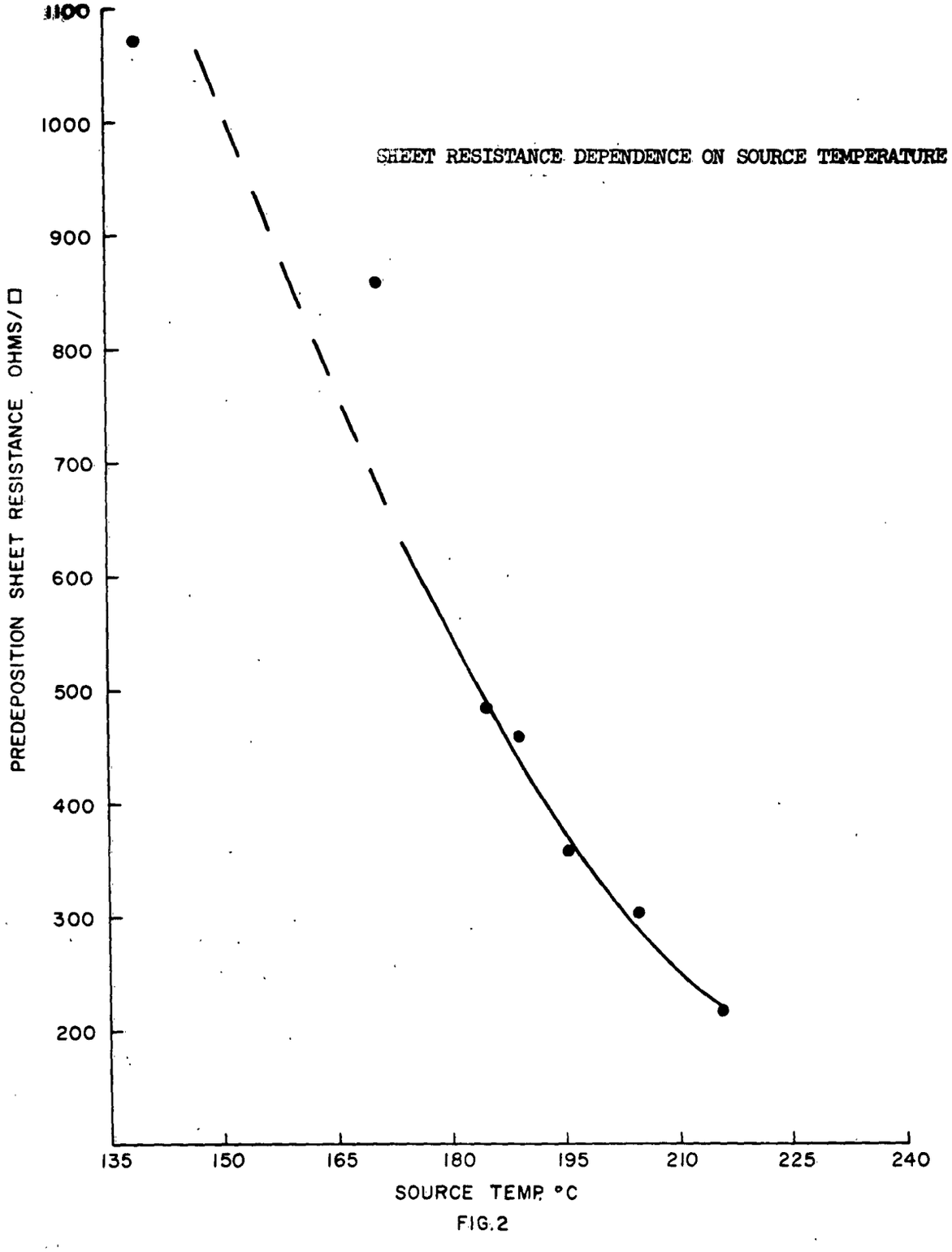

SHEET RESISTANCE DEPENDENCE ON SOURCE TEMPERATURE
PREDEPOSITION SHEET RESISTANCE OHMS/□
1100
1000
900
800
700
600
500
400
300
200
135
150
165
180
195
210
225
240
SOURCE TEMP. °C

FIG.2

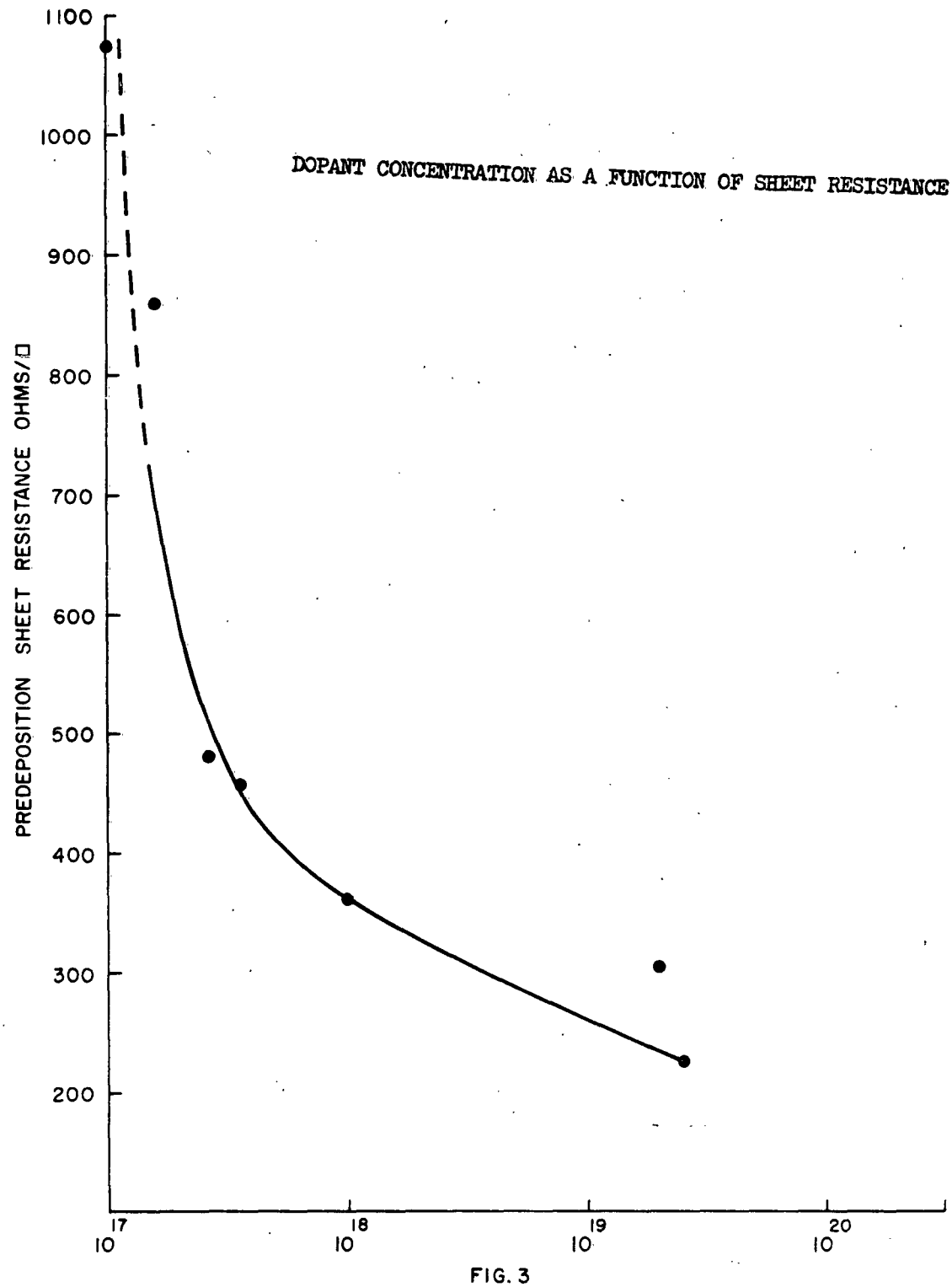
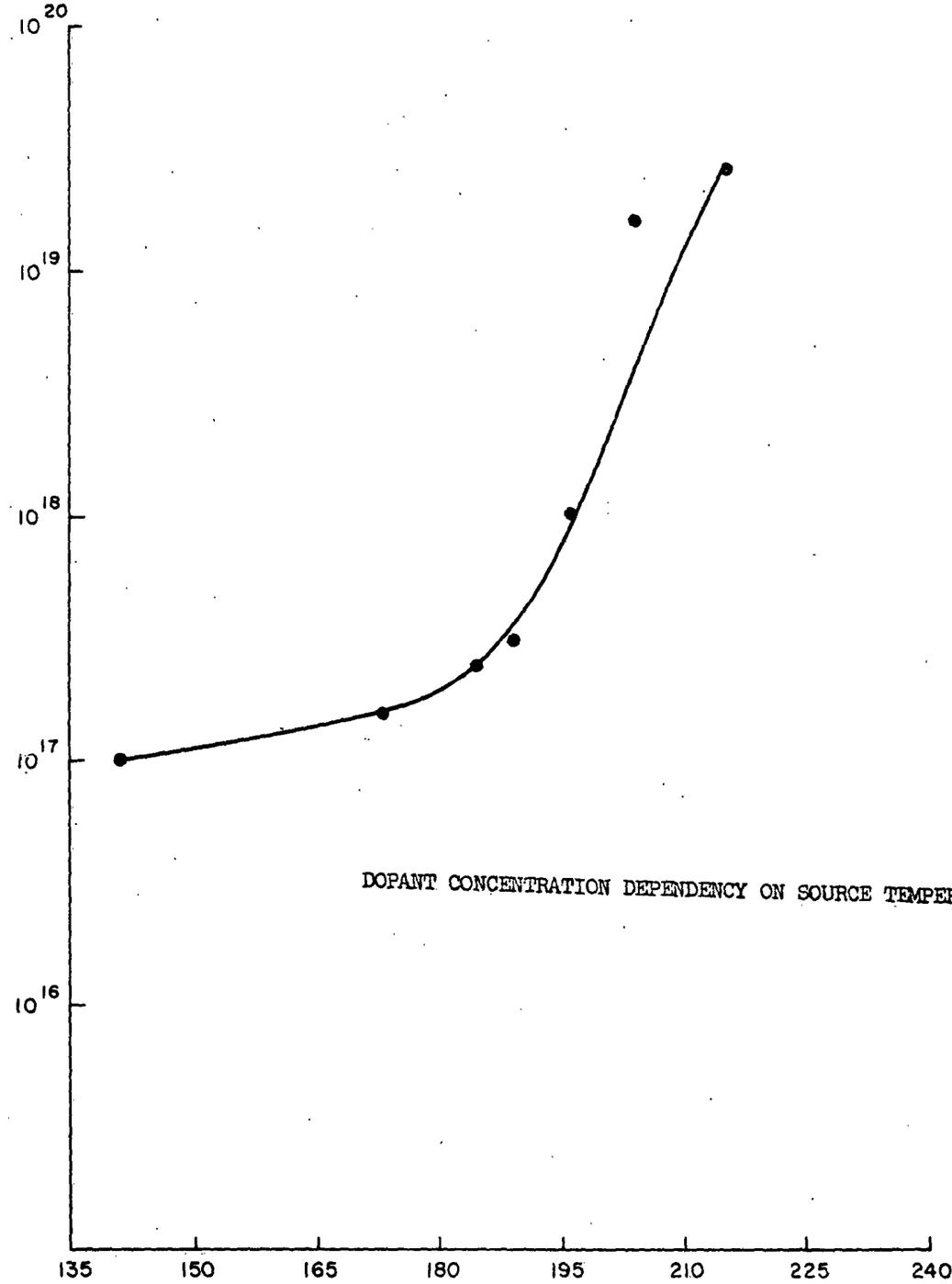

DOPANT CONCENTRATION AS A FUNCTION OF SHEET RESISTANCE
PREDEPOSITION SHEET RESISTANCE OHMS/□
1100
1000
900
800
700
600
500
400
300
200
10^17
10^18
10^19
10^20

FIG. 3



DOPANT CONCENTRATION DEPENDENCY ON SOURCE TEMPERATURE

FIG. 4

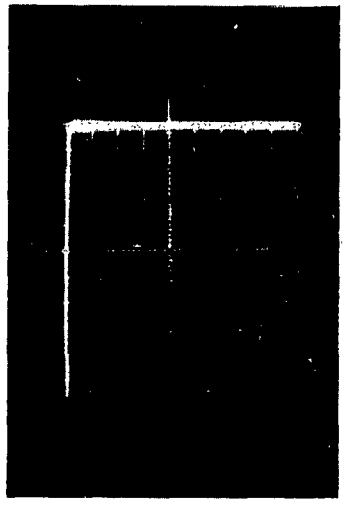


FIG. 5
Abscissa: 10v/div
Ordinate: .01 ma/div

DIODE REVERSE BREAKDOWN

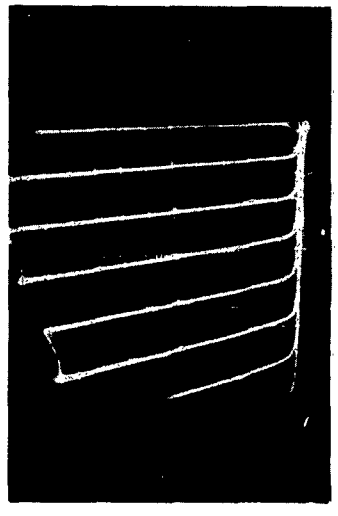


FIG. 6
Abscissa: 2v/div
Ordinate: .5 ma/div
Selector: .01 ma/step

TRANSISTOR CURRENT GAIN

TABLE I

PREDEPOSITION (Time = 1 hr. Wafer temp. = 700°C)		REDISTRIBUTION (Time = 1 hr. Wafer Temp.= 1200°C)		
T source, °C	R_{Sheet}, ohms per square	R_{Sheet}, ohms per square	Junction Depth, microns	Concentration Atoms per cc.
140	1100	225	2.9	9×10^{16}
140	1075	190	3.0	1×10^{17}
140	1050	220	2.8	1
170	850	115	3.1	2
170	875	120	3.0	2
170	845	100	3.1	2
170	855	110	3.1	2
185	450	63	2.9	4
185	475	80	3.0	3.5
185	525	75	2.8	4
185	490	76	2.9	4
185	475	78	3.1	3.5
185	465	74	2.9	4
185	500	80	3.0	3.5
185	490	75	3.0	4
190	490	70	2.8	6
190	450	68	2.8	5
190	445	67	2.8	5
196	360	52	3.0	8
196	350	48	2.9	1×10^{18}
196	370	50	2.8	1
205	335	4.8	2.8	2.5×10^{19}
205	290	4.6	2.7	3
205	320	4.6	2.7	3
205	305	4.5	2.8	3
215	220	3.3	2.9	4
215	225	3.4	2.8	4

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3. Microelectronics, Phosphorous Diffusion for

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II. Army Electronics Research & Development Laboratory, Fort Monmouth, N. J.
III. DA Task 3A99-21-003-01

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